UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Heinen	Group Art Unit:	2857
Application No.:	10/557,104	Examiner:	Charioui, M.
Filed:	27 November 2006	Confirmation No.:	5365
Subject:	INTEGRATED CIRCUIT WITH BIT ERROR TEST CAPABILITY		
Atty Docket No.:	20031035-02		

PLEASE ENTER
MC, 7/2/09

AMENDMENT UNDER 37 CFR 1.116

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Claims 1-13 were presented for examination. In a final Office Action mailed April 3, 2009, Claims 1, 5-8, 10, 12 and 13 were rejected and Claims 2-4, 9 and 11 were objected to.

In response to the final Office Action, Applicants hereby submit an amendment as follows:

A **Claims** listing begins on page 2.
Remarks begin on page 6.